WHAT IS CLAIMED IS:

1. A method for receiving data signals, comprising the steps of:

(1) receiving a data signal having a symbol rate;

(2) generating N sampling signals having a first frequency that is lower than said symbol rate, said N sampling signals shifted in phase relative to one another;

(3) controlling N analog-to-digital converter ("ADC") paths with said N sampling signals to sample said data signal at said phases;

(4) individually adjusting one or more parameters for each of said N ADC paths; and

(5) generating a digital signal representative of said received data signal from samples received from said N ADC paths.

2. The method according to claim 1, wherein step (4) comprises the step of individually adjusting said N sampling signals to reduce phase errors between said received data signal and each of said N sampling signals in said N ADC paths.

3. The method according to claim 2, wherein step (2) comprises the steps of:

(a) generating P clock signals having a second frequency that is approximately equal to said first frequency, said P clock signals shifted in phase relative to one another;

(b) generating N sets of digital control signals; and

(c) weighing said P clock signals under control of each of said set N digital control signals, thereby generating each of said N sampling signals;

wherein step (4) comprises the steps of:

(a) determining phase errors between each of said N sampling signals and said received data signal in each of said N ADC paths; and

(b) individually adjusting said N sets of digital control signals to individually adjust for said phase errors in said N sampling signals.

4. The method according to claim 2, wherein step (2) comprises the steps of:

(a) generating P clock signals having a second frequency approximately equal to said first frequency, said P clock signals shifted in phase relative to one another;

(b) generating N sets of digital control signals; and

(c) interpolating between different sets of said P clock signals under control of said N sets of digital control signals, thereby generating said N sampling signals;

wherein step (4) comprises the steps of:

(a) determining phase errors between each of said N sampling signals and said received data signal in each of said N ADC paths; and

(b) individually adjusting said N sets of digital control signals to individually adjust for said phase errors in the N sampling signals.

5. The method according to claim 1, wherein step (4) comprises the step of individually adjusting for offsets in each of said N ADC paths.

6. The method according to claim 5, wherein step (4) further comprises the step of measuring said offsets in a digital domain and individually adjusting for said offsets in said digital domain for each of said N ADC paths

7. The method according to claim 6, wherein step (4) further comprises the step of measuring said offsets in an M-path parallel decision feedback equalizer ("DFE") and individually adjusting one or more DFE DC taps associated with each of said N ADC paths.

8. The method according to claim 5, wherein step (4) further comprises the step of measuring said offsets in a digital domain and individually adjusting for said offsets in an analog domain for each of said N ADC paths.

9. The method according to claim 8, wherein step (4) further comprises the step of measuring said offsets in an M-path parallel decision feedback equalizer ("DFE") and individually adjusting analog compensation in each of said N ADC paths.

10. The method according to claim 5, wherein step (4) further comprises the step of measuring said offsets in an analog domain and individually adjusting for said offsets in said analog domain for each of said N ADC paths.

11. The method according to claim 1, wherein step (4) comprises the step of individually adjusting for gain errors in said N-ADC paths.

12. The method according to claim 11, wherein step (4) further comprises the step of measuring said gain errors in a digital domain and individually adjusting for said gain errors in said digital domain for each of said N ADC paths.

13. The method according to claim 12, wherein step (4) further comprises the step of measuring said gain errors in an M-path parallel feed-forward equalizer ("FFE") and individually adjusting one or more FFE gain taps associated with each of said N ADC paths.

14. The method according to claim 11, wherein step (4) further comprises the step of measuring said gain errors in a digital domain and individually adjusting for said gain errors in an analog domain for each of said N ADC paths.

15. The method according to claim 14, wherein step (4) further comprises the step of generating digital control signals for each of said N ADC paths and individually adjusting programmable gain amplifiers associated with said N ADC paths under control of said digital control signals.

16. The method according to claim 1, wherein step (4) comprises one or more of the following:

(a) individually adjusting said N sampling signals to reduce phase errors in said N ADC paths;

(b) individually adjusting for offsets in each of said N ADC paths; and

(c) individually adjusting for gain errors in said N-ADC paths.

17. A receiver, comprising:

a receiver input;

an analog-to-digital converter ("ADC") array of N ADC paths, wherein N is an integer greater than 1, each said ADC path including an ADC path input coupled to said receiver input;

an M-path DSP coupled to said ADC array, wherein M=kN and k is an integer or a number in the form of 1/s, where s is an integer;

said M-path DSP having a timing recovery module, wherein said timing recovery module recovers N sampling clocks from a data signal received at said receiver input, said data signal having a baud frequency, said N sampling clocks having a first frequency that is N times lower than said baud frequency, said N sampling clocks being shifted in phase relative to one another, whereby said timing recovery module provides said N sampling

clocks to said N ADC paths, whereby said N sampling clocks control said N ADC paths to sample said received signal at said phases; and

means for individually adjusting one or more parameters for each of said N ADC paths.

18. The receiver according to claim 17, wherein said means for individually adjusting one or more parameters for each of said N ADC paths comprises means for individually adjusting each of said N sampling signals to reduce sampling phase errors in said N ADC paths.

19. The receiver according to claim 18, wherein said means for individually adjusting one or more parameters for each of said N ADC paths comprises N timing recovery loops within said timing recovery module, each of said N timing recovery loops including an output coupled to a corresponding one of said N ADC paths, whereby each said timing recovery loop determines a sampling phase error in said corresponding one of said N ADC paths and individually adjusts a corresponding one of said N sampling signals to reduce said sampling phase error.

20. The receiver according to claim 19, further comprising:

a frequency divider that outputs P clock signals having a second frequency that is approximately equal to said first frequency and with substantially equal phase differences between said P clock signals, wherein P is at least 3; and

a phase interpolator that includes P phase inputs, wherein said phase interpolator generates said N sampling clocks from said P clock signals, wherein N need not equal to P, wherein each said timing recovery loop generates a phase interpolator control signal, said phase interpolator including N phase adjusters whereby each said N phase adjuster adjusts a phase of a corresponding one of said N sampling clocks under control of a corresponding

one of said timing recovery loop phase interpolator control signals to reduce said sampling phase error in a corresponding one of said ADC paths.

21. The receiver according to claim 20, wherein P is greater than N.

22. The receiver according to claim 20, wherein P is less than N.

23. The receiver according to claim 20, wherein said phase interpolator comprises a digital-to-analog converter ("DAC").

24. The receiver according to claim 23, wherein said phase interpolator control signals are digital phase interpolator control signals and wherein each of said N phase adjusters comprises:

a digital decoder coupled to a corresponding one of said N timing recovery loops;

P digital-to-analog converters, each coupled to said decoder;

means for weighting each of said P clock signals under control of said P digital-to-analog converters; and

means for summing outputs of said means for weighting, whereby an output of said means for summing is one of said N sampling clock outputs.

25. The receiver according to claim 24, wherein said means for weighting comprises P differential pairs of NMOS transistors, each said pair of NMOS transistors having gate terminals coupled to a corresponding differential pair of one of said P phases, source terminals coupled to a corresponding one of said digital-to-analog converters, and drain terminals coupled to said means for summing.

26. The receiver according to claim 20, wherein said phase interpolator comprises a resistive interpolation ring.

27. The receiver according to claim 18, wherein k is an integer greater than 1, said M-path DSP including N sets of k inputs, each of said N sets of k inputs coupled to an output of a corresponding one of said N ADC paths.

28. The receiver according to claim19, wherein:

k is an integer;

each of said M DSP paths include k decision generators and k slicer error generators, wherein said decision generator outputs decisions for a corresponding DSP path and said error generator outputs slicer errors for said corresponding DSP path; and

each said timing recovery loop includes k phase detectors, each said phase detector including decision and error inputs coupled to decision and error outputs of said DSP paths, whereby said k phase detectors determine phase differences between said input data signal and a local reference clock, each said timing recovery loop including a summer having inputs coupled to outputs of said k phase detectors, whereby said summers add the phase differences determined by said phase detectors, each said timing recovery loop including a phase locked loop having an input coupled to an output of said summer, whereby said phase locked loops generate said phase interpolator control signals to minimize corresponding phase differences between said input data signal and said local reference clock.

29. The receiver according to claim 28, wherein k is equal to one, M equals N, and M and N are greater than 1, and wherein:

each of said M DSP paths include a decision generator and a slicer error generator; and

each of said N timing recovery loops include a phase detector, each said phase detector including a decision input coupled to a corresponding DSP path decision generator output, each said phase detector including a slicer

error input coupled to a DSP path slicer error generator output in a DSP path adjacent to said corresponding DSP path.

30. The receiver according to claim 28, wherein:

k is equal to two, N equals 4, and M equals 8;

said four ADC paths consecutively sample a received data signal at approximately 90 degree phase intervals;

each said M DSP path includes two decision generators and two slicer error generators;

each said timing recovery loop includes first and second phase detectors, wherein;

said first phase detector of a first one of said N timing recovery loops is coupled to a decision generator output of a first one of said M DSP paths and to a slicer error generator output of an eighth one of said DSP paths;

said second phase detector of said first timing recovery loop is coupled to a decision generator output of a fifth one of said M DSP paths and to a slicer error generator output of a fourth one of said M DSP paths;

said first phase detector of a second one of said N timing recovery loops is coupled to a decision generator output of a second one of said M DSP paths and to a slicer error generator output of said first DSP path;

said second phase detector of said second timing recovery loop is coupled to a decision generator output of a sixth one of said M DSP paths and to a slicer error generator output of said fifth DSP path;

said first phase detector of a third second one of said N timing recovery loops is coupled to a decision generator output of a third one of said M DSP paths and to a slicer error generator output of said second DSP path;

said second phase detector of said third timing recovery loop is coupled to a decision generator output of a seventh one of said M DSP paths and to a slicer error generator output of said sixth DSP path;

said first phase detector of a fourth one of said N timing recovery loops is coupled to a decision generator output of said eighth DSP path and to a slicer error generator output of said seventh DSP path; and

said second phase detector of said fourth timing recovery loop is coupled to a decision generator output of said fourth DSP path and to a slicer error generator output said third DSP path.

31. The receiver according to claim 17, wherein said means for individually adjusting one or more parameters for each of said N ADC paths comprises means for individually adjusting for offsets in said N ADC paths.

32. The receiver according to claim 31, wherein said means for individually adjusting for offsets in said N ADC paths comprises digital measuring means for measuring said offsets and digital adjusting means for individually adjusting for said offsets.

33. The receiver according to claim 32, wherein said digital measuring means comprises an M-path parallel decision feedback equalizer ("DFE") in said M-path DSP, and said digital adjusting means comprises one or more DFE DC taps associated with each of said N ADC paths.

34. The receiver according to claim 31, wherein said means for individually adjusting for offsets in said N ADC paths comprises digital measuring means for measuring said offsets and analog adjusting means for individually adjusting for said offsets.

35. The receiver according to claim 34, wherein said digital measuring means comprises an M-path parallel decision feedback equalizer ("DFE") in said M-path DSP, and said analog adjusting means comprises means for individually adjusting analog compensation in each of said N ADC paths.

36. The receiver according to claim 31, wherein said means for individually adjusting for offsets in said N ADC paths comprises analog measuring means for measuring said offsets and analog adjusting means for individually adjusting for said offsets.

37. The receiver according to claim 17, wherein said means for individually adjusting one or more parameters for each of said N ADC paths comprises means for individually adjusting for gain errors in said N ADC paths.

38. The receiver according to claim 37, wherein said means for individually adjusting for gain errors in said N ADC paths comprises digital measuring means for measuring said gain errors and digital adjusting means for individually adjusting for said gain errors.

39. The receiver according to claim 38, wherein said digital measuring means comprises an M-path parallel feed-forward equalizer ("FFE") in said M-path DSP, and said digital adjusting means comprises one or more FFE gain taps associated with each of said N ADC paths.

40. The receiver according to claim 37, wherein said means for individually adjusting for gain errors in said N ADC paths comprises digital measuring means for measuring said gain errors and analog adjusting means for individually adjusting for said gain errors.

41. The receiver according to claim 40, wherein said analog adjusting means comprises N programmable gain amplifiers, each said programmable gain amplifier associated with a corresponding one of said N ADC paths.

42. The receiver according to claim 17, wherein said means for individually adjusting one or more parameters for each of said N ADC paths comprises one or more of the following:

means for individually adjusting each of said N sampling signals to reduce sampling phase errors in said N ADC paths;

means for individually adjusting for offsets in said N ADC paths; and

means for individually adjusting for gain errors in said N ADC paths.

43. The method according to claim 1, wherein step (4) comprises generating a decision-directed error signal, and step (5) comprises individually adjusting one or more parameters for each of said N ADC paths to reduce said decision-directed error signal.

44. The method according to claim 43, wherein step (4) further comprises generating a decision with a slicer and subtracting said decision from said samples.

45. The method according to claim 43, wherein step (4) further comprises providing a decision from a Viterbi detector to a channel estimator, and subtracting an output from said channel estimator from said samples.

46. The method according to claim 45, wherein step (4) further comprises providing a tentative decision from a Viterbi detector to said channel estimator.

47. The method according to claim 45, wherein step (4) further comprises providing a final decision from a Viterbi detector to said channel estimator.

48. The method according to claim 1, wherein step (4) comprises generating a non-decision-directed error signal, and step (5) comprises individually adjusting one or more parameters for each of said N ADC paths to reduce said non-decision-directed error signal.

49. The method according to claim 2, wherein step (5) further comprises using a feed-forward equalizer as a phase interpolator to individually adjust said N sampling signals.

50. The method according to claim 1, wherein step (4) comprises performing an equalization process to compensate for one or more of:

cross-talk;
inter-symbol interference;
attenuation; and
noise.

51. The apparatus according to claim 17, wherein said means for individually adjusting one or more parameters for each of said N ADC paths comprises:

a decision-directed error signal generator that generates a decision-directed error signal; and

at least one adaptive processor that adjusts said one or more parameters to reduce said decision-directed error signal.

52. The apparatus according to claim 51, wherein said decision-directed error signal generator comprises a slicer that receives samples of said received signal, and a subtractor that subtracts decisions from said slicer from said samples, wherein said subtractor outputs said decision-directed error signal.

53. The apparatus according to claim 51, wherein said decision-directed error signal generator comprises a Viterbi decoder that receives samples of said received signal, a channel estimator that receives decisions from said Viterbi decoder, and a subtractor that subtracts an output of said channel estimator from said samples, wherein said subtractor outputs said decision-directed error signal.

54. The apparatus according to claim 53, wherein said channel estimator receives final decisions from said Viterbi decoder.

55. The apparatus according to claim 53, wherein said channel estimator receives tentative decisions from said Viterbi decoder.

56. The apparatus according to claim 17, wherein said means for individually adjusting one or more parameters for each of said N ADC paths comprises:

a non-decision-directed error signal generator that generates a non-decision-directed error signal; and

at least one adaptive processor that adjusts said one or more parameters to reduce said non-decision-directed error signal.

57. The apparatus according to claim 18, wherein said means for individually adjusting each of said N sampling signals comprises a feed-forward equalizer implemented as a phase interpolator to individually adjust said N sampling signals.

58. The apparatus according to claim 17, wherein said M-path DSP comprises an equalizer configured to compensate for one or more of:

cross-talk;
inter-symbol interference;
attenuation; and
noise.

59. The method according to claim 1, further comprising performing one or more digital processes on said samples and generating control signals from said one or more digital processes, wherein said control signals are used to perform said individually adjusting step (4).

60. The method according to claim 1, further comprising performing one or more M-path parallel digital processes on said samples, wherein M=kN, and k is an integer or a number in the form of 1/s, where s is an integer, and generating control signals from said one or more M-path parallel digital processes, wherein said control signals are used to perform said individually adjusting step (4).

61. A method for receiving data signals, comprising the steps of:

(1) receiving a data signal having a symbol rate;

(2) generating N sampling signals having a first frequency that is lower than said symbol rate, said N sampling signals shifted in phase relative to one another;

(3) controlling N analog-to-digital converter ("ADC") paths with said N sampling signals to sample said data signal at said phases;

(4) performing one or more digital processes on samples from said N ADC paths and generating control signals from said one or more digital processes;

(5) individually adjusting one or more parameters for each of said N ADC paths using said control signals; and

(6) generating a digital signal representative of said received data signal.

62. A method for receiving data signals, comprising the steps of:

(1) receiving a data signal having a symbol rate;

(2) generating N sampling signals having a first frequency that is lower than said symbol rate, said N sampling signals shifted in phase relative to one another;

(3) controlling N analog-to-digital converter ("ADC") paths with said N sampling signals to sample said data signal at said phases;

(4) performing one or more M-path parallel digital processes on samples from said N ADC paths, wherein M=kN, and k is an integer or a number in the form of 1/s, where s is an integer, and generating control signals from said one or more M-path parallel digital processes;

(5) individually adjusting one or more parameters for each of said N ADC paths using said control signals; and

(6) generating a digital signal representative of said received data signal.

63. A method for receiving data signals, comprising the steps of:

(1) receiving a data signal having a symbol rate;

(2) generating N sampling signals having a first frequency that is lower than said symbol rate, said N sampling signals shifted in phase relative to one another;

(3) controlling N analog-to-digital converter ("ADC") paths with said N sampling signals to sample said data signal at said phases;

(4) individually adjusting one or more parameters for each of said N ADC paths, including individually adjusting at least a sampling phase in each of said N ADC paths to compensate for phase errors between each said N sampling signals and said received data signal; and

(5) generating a digital signal representative of said received data signal from samples received from said N ADC paths.

64. A receiver, comprising:

a receiver input;

an analog-to-digital converter ("ADC") array of N ADC paths, wherein N is an integer greater than 1, each said ADC path including an ADC path input coupled to said receiver input;

an M-path DSP coupled to said ADC array, wherein M=kN and k is an integer or a number in the form of 1/s, where s is an integer; and

said M-path DSP having a timing recovery module, wherein said timing recovery module recovers N sampling clocks from a data signal received at said receiver input, said data signal having a baud frequency, said N sampling clocks having a first frequency that is N times lower than said baud frequency, said N sampling clocks being shifted in phase relative to one another, whereby said timing recovery module provides said N sampling clocks to said N ADC paths, whereby said N sampling clocks control said N ADC paths to sample said received signal at said phases.

65. A method for receiving data signals, comprising the steps of:

(1) receiving a data signal having a symbol rate;

(2) generating N sampling signals having a first frequency that is lower than said symbol rate, said N sampling signals shifted in phase relative to one another;

(3) controlling N analog-to-digital converter ("ADC") paths with said N sampling signals to sample said data signal at said phases;

(4) performing one or more digital processes on samples from said N ADC paths and generating control signals from said one or more digital processes;

(5) individually adjusting one or more parameters for each of said N ADC paths using said control signals, including individually adjusting at least a sampling phase in each of said N ADC paths to compensate for phase errors between each said N sampling signals and said received data signal; and

(6) generating a digital signal representative of said received data signal.

66. A method for receiving data signals, comprising the steps of:

(1) receiving a data signal having a symbol rate;

(2) generating N sampling signals having a first frequency that is lower than said symbol rate, said N sampling signals shifted in phase relative to one another;

(3) controlling N analog-to-digital converter ("ADC") paths with said N sampling signals to sample said data signal at said phases;

(4) performing one or more M-path parallel digital processes on samples from said N ADC paths, wherein M=kN, and k is an integer or a number in the form of 1/s, where s is an integer, and generating control signals from said one or more M-path parallel digital processes;

(5) individually adjusting one or more parameters for each of said N ADC paths using said control signals, including individually adjusting at least a sampling phase in each of said N ADC paths to compensate for phase errors between each said N sampling signals and said received data signal; and

(6) generating a digital signal representative of said received data signal.